UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/866,656	05/30/2001	Sung-Il Park	8733.434.00	5149

30827 7590 06/18/2003

MCKENNA LONG & ALDRIDGE LLP
1900 K STREET, NW
WASHINGTON, DC 20006

EXAMINER
QI, ZHI QIANG

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 06/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/866,656	PARK ET AL.	
	Examiner	Art Unit	
	Mike Qi	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-21 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-21 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1, recitation" . . . wherein one of the gate transmitting line has a resistance of below 30 Ω and is capable of transmitting a gate low voltage." is indefinite. Because the gate transmitting line is capable of transmitting a gate low voltage that indicates the gate transmitting line can or may transmit a gate low voltage, but it does not indicate the definite function of the gate transmitting line. For examination purpose, it is interpreted as the gate transmitting line serves as transmitting the scanning signal such as a scanning waveform signal.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant admitted prior art (AAPA) in view of US 5,748,179 (Ito et al) and US 5,739,880 (Suzuki et al).

Claims 1, 14, 20 and 21, AAPA discloses (paragraph 0002 – 0028; Figs.1-6) that generally, a liquid crystal display device having a liquid crystal panel comprising:

(concerning claims 1, 14 and 20)

- a first (lower) substrate (20), a second (upper) substrate (10), the first (lower) substrate (20) having a plurality of source pads (30 of Figs.3 - 4) and gate pads (28 of Figs.3 - 4) (because the FPC 40 as the gate transmitting lines formed on the lower substrate 20), and the first (lower) and second (upper) substrates (20, 10) being attached;
- a first printed circuit board (source PCB 33) connected to the plurality of source pads (30 of Fig.4), and the source PCB (33) applying signals to the source pads (30 of Fig.4);
- a second printed circuit board (gate PCB 31) connected to the plurality of gate pads (28 of Fig.4), and the gate PCB (31) applying signals to the gate pads (28 of Fig.4);
- a plurality of gate transmitting lines (FPC 40 transmits the gate signals) formed directly on the lower substrate (20) and connecting the gate pads (28 of Fig.4) with the source pads (30 of Fig.4), the plurality of gate transmitting lines (FPC 40) transmitting signals from the source PCB (33) to the gate PCB (31) via the gate transmitting lines (FPC 37 or 40);

(concerning claims 1 and 21) (Claim 21 also has a same deficiency as the claim 1 as the explanation under 35 U.S.C. 112 rejection above.)

- the gate transmitting lines (FPC 40) transmits the gate signals, inherently, one of the gate transmitting lines transmits a gate voltage signal, and that must include a gate low voltage scanning signal.

The AAPA discloses all the limitations as claimed in claims 14 and 20. The AAPA does not expressly disclose one of the gate transmitting lines has a resistance of below 30 Ω as claimed in claim 1 and in claim 21.

However, Ito discloses (col.7, line 56 – col.8, line 13; Fig.5) that the resistance value from the connection portion of the input wire (Td) with the flexible board to the input terminal (Ip) is equal to several ohms. Further, the input terminal portion itself is required to have a resistance value of several ohms. Therefore, the signal transmitting lines in LCD are required to have a resistance value of several ohms that is below 30 ohms.

Ito also indicates (col.16, lines 17 – 34) that larger resistance occurs at the gate side and at the drain side would cause the distortion amount of the output waveform of the driving IC is varied every wiring, and this finally causes unevenness of a display image. Therefore, it is necessary to reduce the resistance of the signal transmitting lines in order to reduce the signal distortion such as a cross-talk.

Further, Suzuki discloses (col.12, lines 5-27; Fig.7) that it is necessary to reduce the resistance of the output wiring (i.e., the signal transmitting lines), because the signal waveform propagation delay is dependent on the resistance of the signal transmitting

lines such as the gate lines and the capacitance loaded upon the signal transmitting lines such as the gate lines (i.e., the RC constant). Therefore, the larger resistance of the signal transmitting line would cause larger signal propagation delay, and that would cause signal waveform distortion, and unevenness of a display image.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to arrange one of the gate transmitting lines having a resistance of below 30 ohms as claimed in claims 1, 14, 20 and 21 for preventing the unevenness of a display image, i.e., to reduce the resistance of the signal transmitting lines in order to reduce the signal distortion such as a cross-talk.

Claims 2 and 15, AAPA discloses (paragraph 0019; Figs. 3 - 4) that the plurality of gate transmitting lines (40) include at least eight signal lines for transmitting signals from the source PCB (33) to the gate PCB (31).

Claims 3-9 and 16-17, AAPA discloses (paragraph 0015, 0019) that the gate transmitting lines (FPC 37 or 40 transmits the gate signals) include Vcom (common voltage signal line); Vgh (gate high voltage signal line); Vgl (gate low voltage signal line); Gsc and Goe (to control the signal passing through the gate line); Gsp (to control the drive IC); Vcc (power line) and Vdd (ground line).

Claims 10-12 and 18-19, AAPA discloses (paragraph 0020) that dummy pads are preferably formed in gaps between adjacent gate pads (28) and between adjacent source pads (30), so as to prevent an abnormal electrical interaction between the adjacent gate transmitting wires, and that would have been at least obvious.

Claim 13, AAPA discloses (paragraph 0017; Fig.3) that a plurality of connecting wires (i.e., the FPC 40 transmitting gate signals as the gate transmitting lines) are formed directly on the lower substrate (20).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mike Qi whose telephone number is (703) 308-6213. .

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Mike Qi
May 23, 2003

T. Chowdhury
Primary Examiner